IBM Research

Tailoring performance of nanoelectronics using strain engineering

Conal E. Murray
IBM T.J. Watson Research Center

conal@us.ibm.com

10/24/2017

Outline

Motivation

- link between mechanical response and device performance
- measurement techniques

Strain distributions in Si-based technology

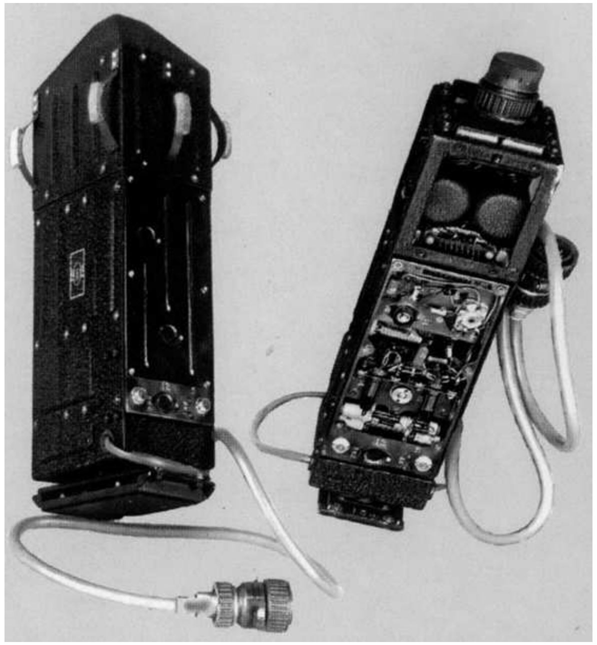
- elastic anisotropy
- effects of feature geometry on device channel strain

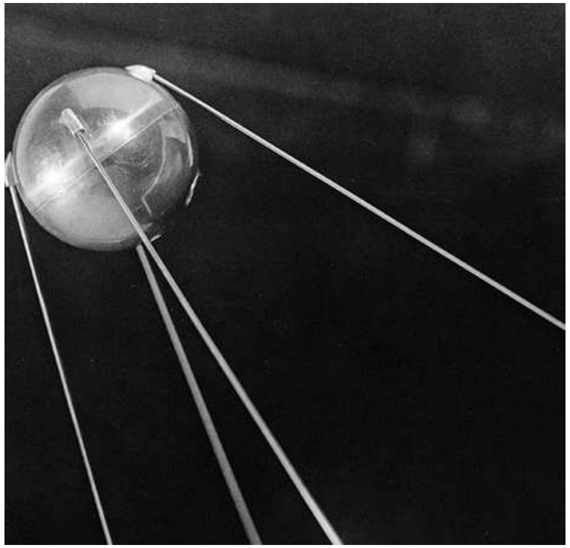
Depth-dependent strain distributions in metallization

- constraint of plastic relaxation

Summary and Conclusions

Reaching new heights





en.wikipedia.org/wiki/Sputnik_1

Sputnik 1:
- 1 W transmitter (20, 40 MHz)

Apollo GC:
- 1.024 MHz, 64 KB

en.wikipedia.org/Wiki/
Apollo_Guidance_Computer

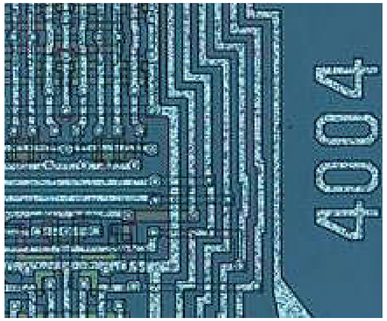
Motivation

Nanomaterials:

- new properties enabled by increasing surface to volume ratio
  - ➢ strength
  - ➢ electronic behavior
  - ➢ interfaces are everywhere

- semiconductor device scaling
  - ✓ increased density
  - ✗ lithographic scaling is no longer sufficient in improving device performance

➢ new materials and geometries must be incorporated



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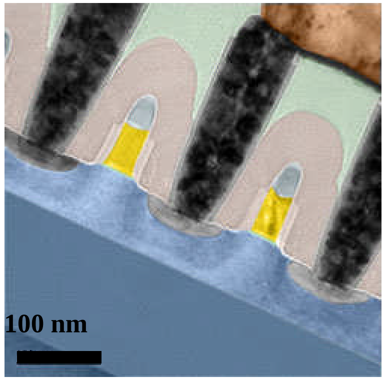
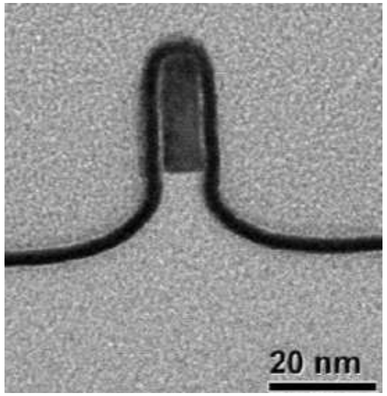
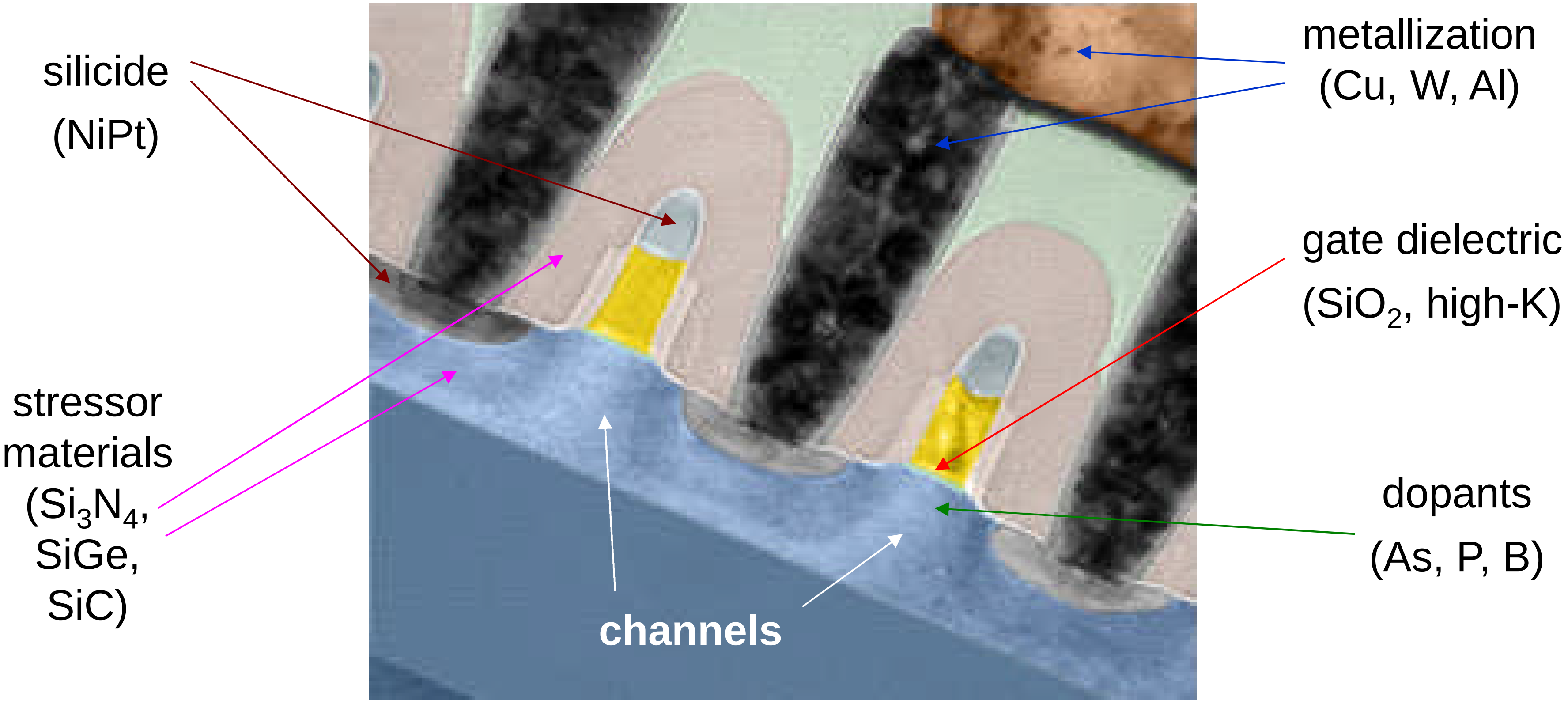




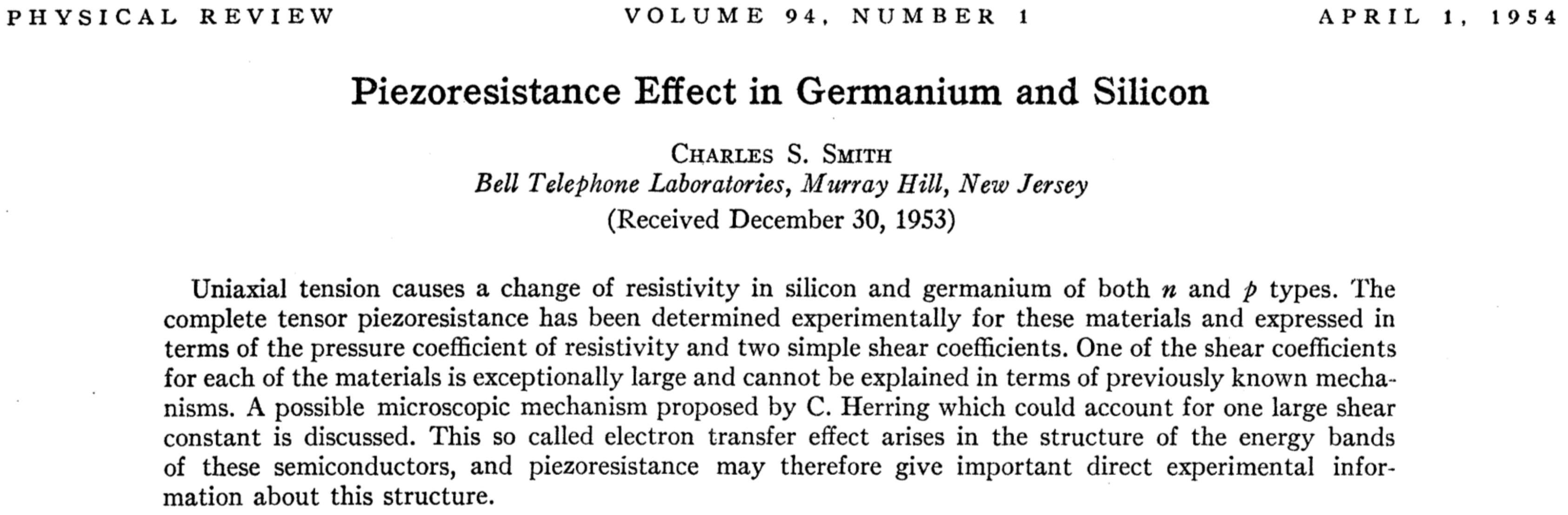
P. Hashemi et al.,
ECS Trans. **75**, 39 (2016)

Issues associated with device performance

- strained Si channels lead to enhanced carrier mobility in devices
- composition, phase transitions, and microstructure of device components
- mechanical behavior and interfacial scattering within devices



CMOS technology improvements → beyond scaling



PHYSICAL REVIEW VOLUME 94, NUMBER 1 APRIL 1, 1954

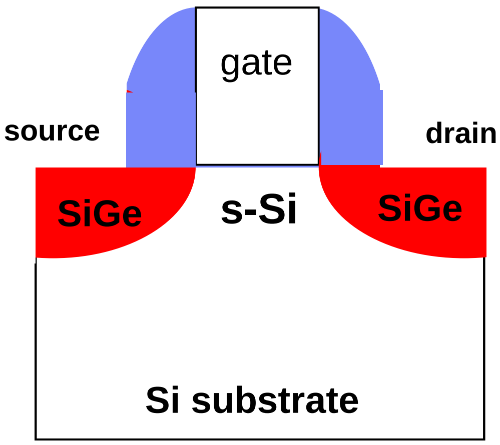
Piezoresistance Effect in Germanium and Silicon

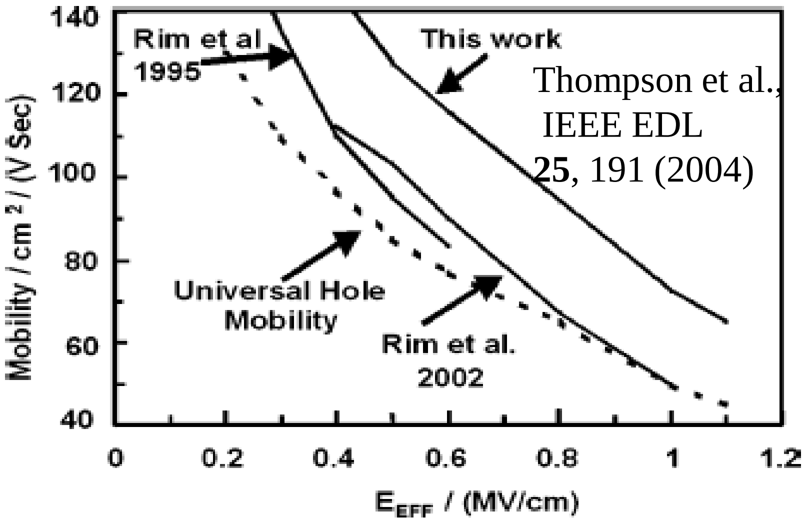
CHARLES S. SMITH
Bell Telephone Laboratories, Murray Hill, New Jersey

(Received December 30, 1953)

Uniaxial tension causes a change of resistivity in silicon and germanium of both *n* and *p* types. The complete tensor piezoresistance has been determined experimentally for these materials and expressed in terms of the pressure coefficient of resistivity and two simple shear coefficients. One of the shear coefficients for each of the materials is exceptionally large and cannot be explained in terms of previously known mechanisms. A possible microscopic mechanism proposed by C. Herring which could account for one large shear constant is discussed. This so called electron transfer effect arises in the structure of the energy bands of these semiconductors, and piezoresistance may therefore give important direct experimental information about this structure.

- ➢ **carrier mobility enhancement through strain engineering**





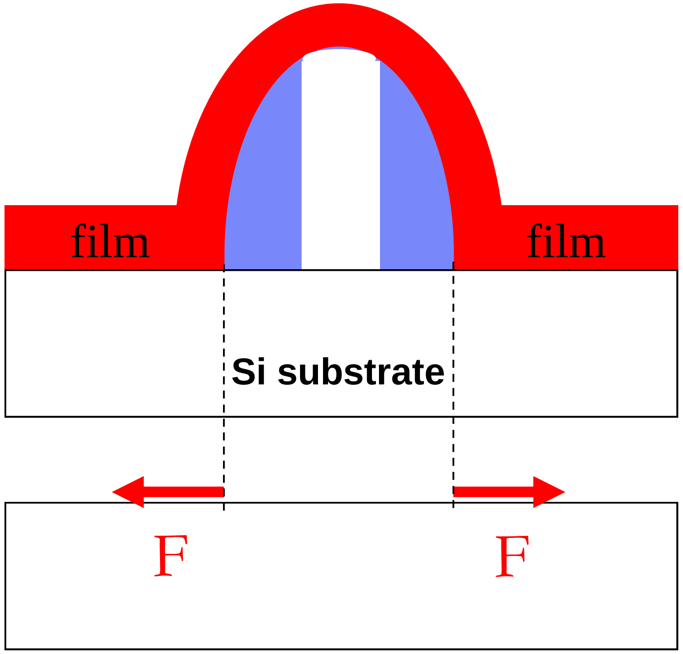
Thompson et al., IEEE EDL **25**, 191 (2004)

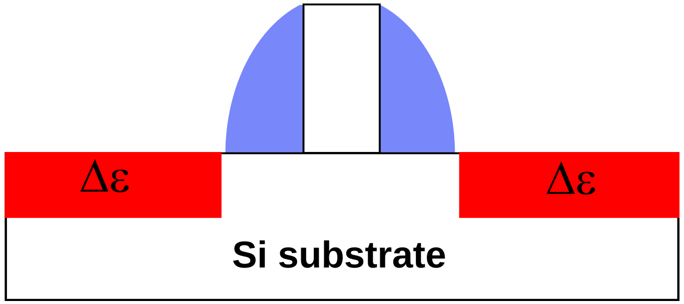
Methods to strain Si

- **Stressed liner materials:**
  - discontinuities in overlying features
  - spacer / gate structures produce edges
  - same sign of strain induced in channel

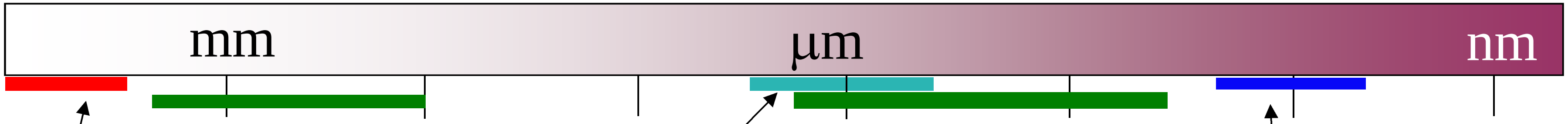
- **Embedded strained features:**
  - in-plane “uniaxial” loading of channel
  - lattice-mismatched material (Δε)
  - Si(Ge) → compressive strain
  - Si(C) → tensile strain

- **Variation in piezoresistive coefficients:**
  - device layout (edge effects) will impact strain
  - need a method to quantify stress induced in Si





Looking at strain in CMOS technology



- **Wafer curvature**
  - ➢ in-plane stress
  - ➢ ~ MPa·µm resolution (Si wafer)
  - ✗ uniform, perfect adhesion

- **Raman**
  - ✓ amorphous and crystalline materials
  - ➢ strain resolution ~ high 10^{-5}
  - ✗ hard to interpret triaxial stress states
  - ✗ sensitive to temperature (self-heating)

- **XRD**
  - ➢ macro and microbeam
  - ✓ *in-situ*, direct measurements of lattice spacing
  - ✓ strain resolution ~ mid 10^{-5}
  - ➢ large penetration depth

- **TEM**
  - ✓ superior spatial resolution NBD ~ 10 nm, DF holo. ~ 5 nm
  - ➢ strain resolution ~ mid 10^{-4}
  - ✗ relaxation due to sample prep.

Mechanical response of strained films

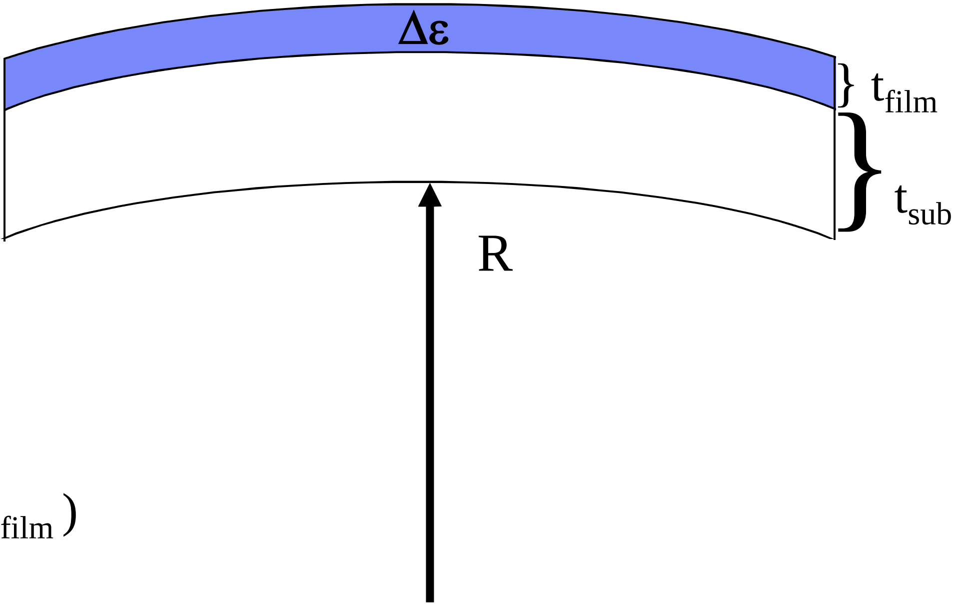
Blanket films:

- radius of curvature, R, related to biaxial film stress, $\sigma_{film} = \Delta\varepsilon\, E_{film}/(1-\nu_{film})$
- force and moment balance between thin film and substrate
- assumes uniform stress throughout film
- ➢ no lateral dependence of stress, film thickness, modulus (E), adhesion

Timoshenko

- ➢ J. Opt. Soc. Am. **11**, 233, (1925)

$$\sigma_{film} = \frac{1}{6} \cdot \frac{\left(E_{film} t_{film}^3 + E_{sub} t_{sub}^3\right)}{R\, t_{film}\left(t_{film} + t_{sub}\right)}$$



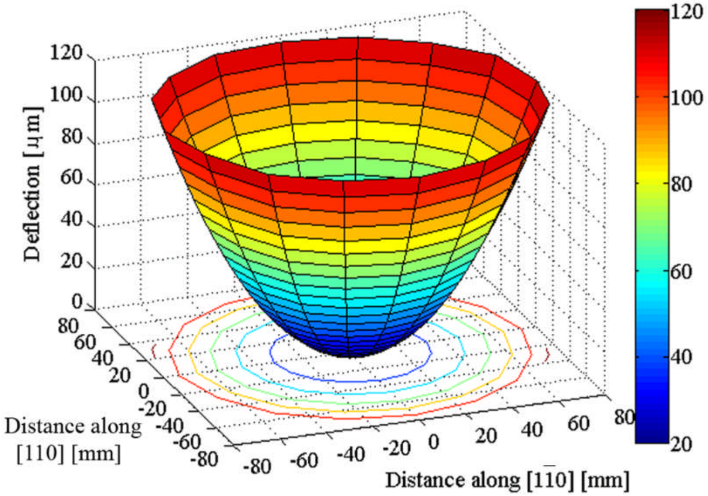
Stoney

- ➢ Proc. Roy. Soc. Lon. A **82**, 172 (1909)

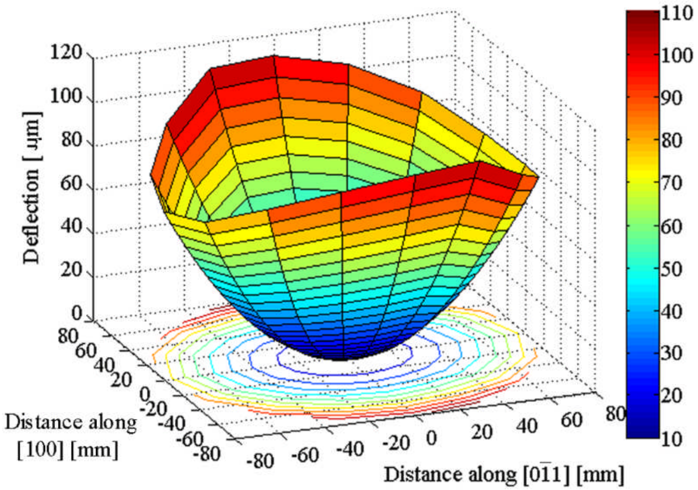
$$\sigma_{film} \approx \frac{E_{sub}}{6} \cdot \frac{t_{sub}^2}{R\, t_{film}} \qquad (t_{sub} >> t_{film})$$

Effects of substrate anisotropy on curvature

505 nm thick Si_3N_4 film on Si (001)

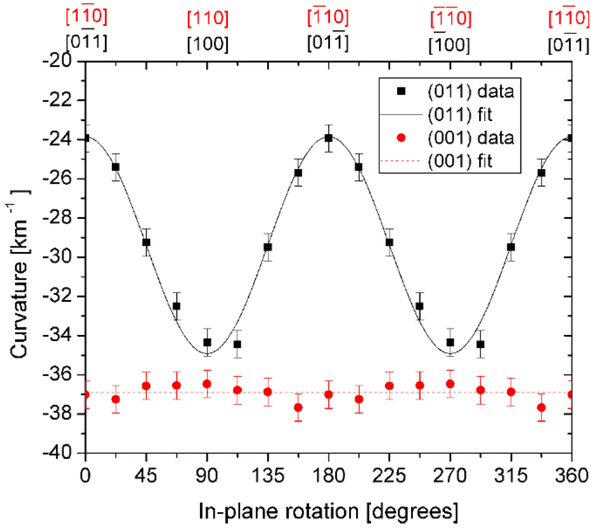


501 nm thick Si_3N_4 film on Si (011)



Neumann's principle:

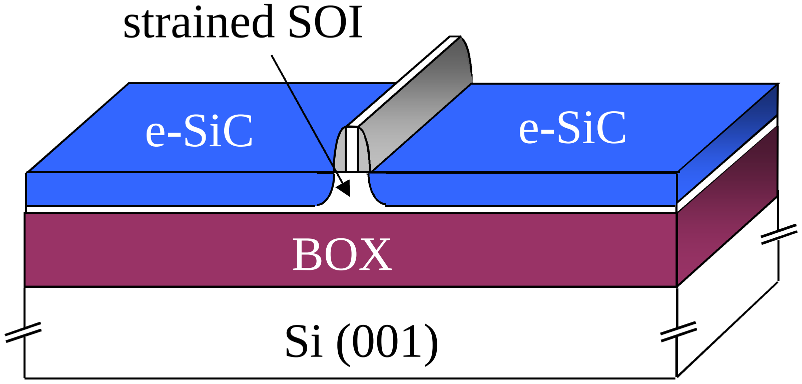
- 2-fold symmetry → two principal curvatures
- 3-fold or 4-fold symmetry → isotropic



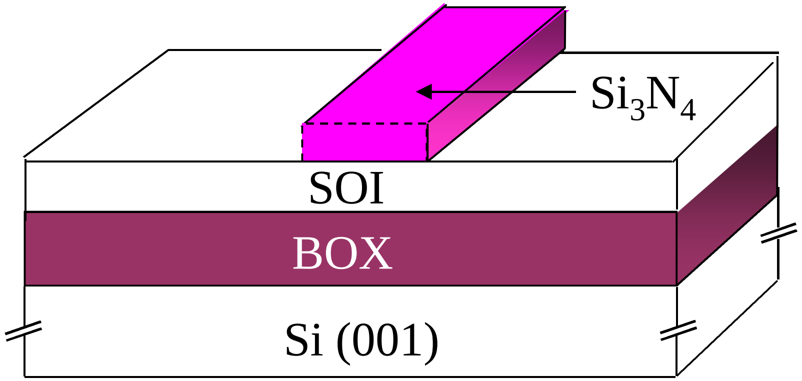
C.E. Murray & K.L. Saenger, J. Appl. Phys. **104**, 103509 (2008)

XRD microbeam measurements of strained Si

Embedded Stressors



Stressed Liners



- ➢ assess efficacy of strain transfer to silicon-on-insulator (SOI) channel regions

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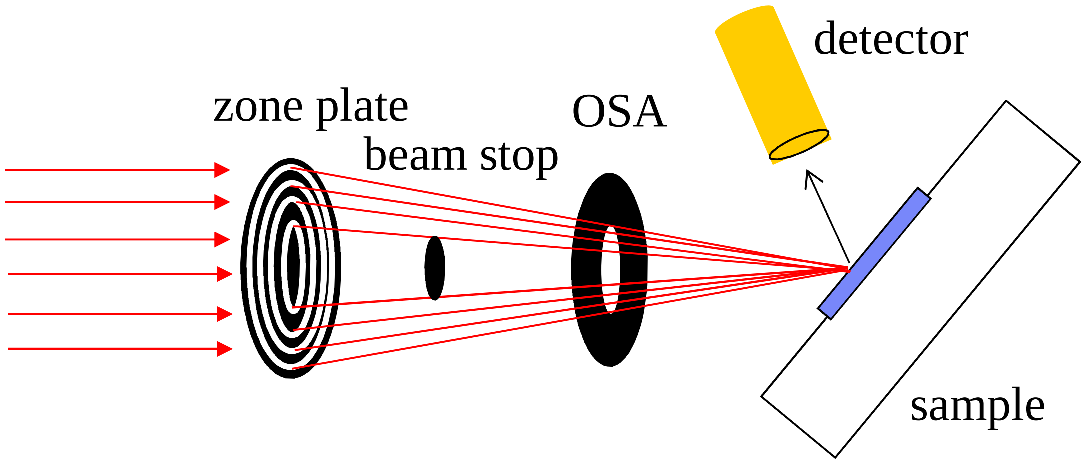
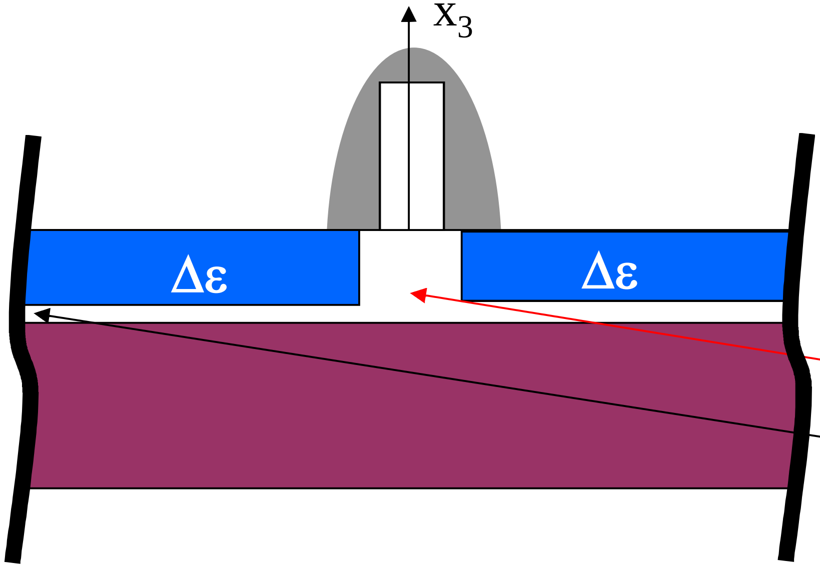
APS 2ID-D:

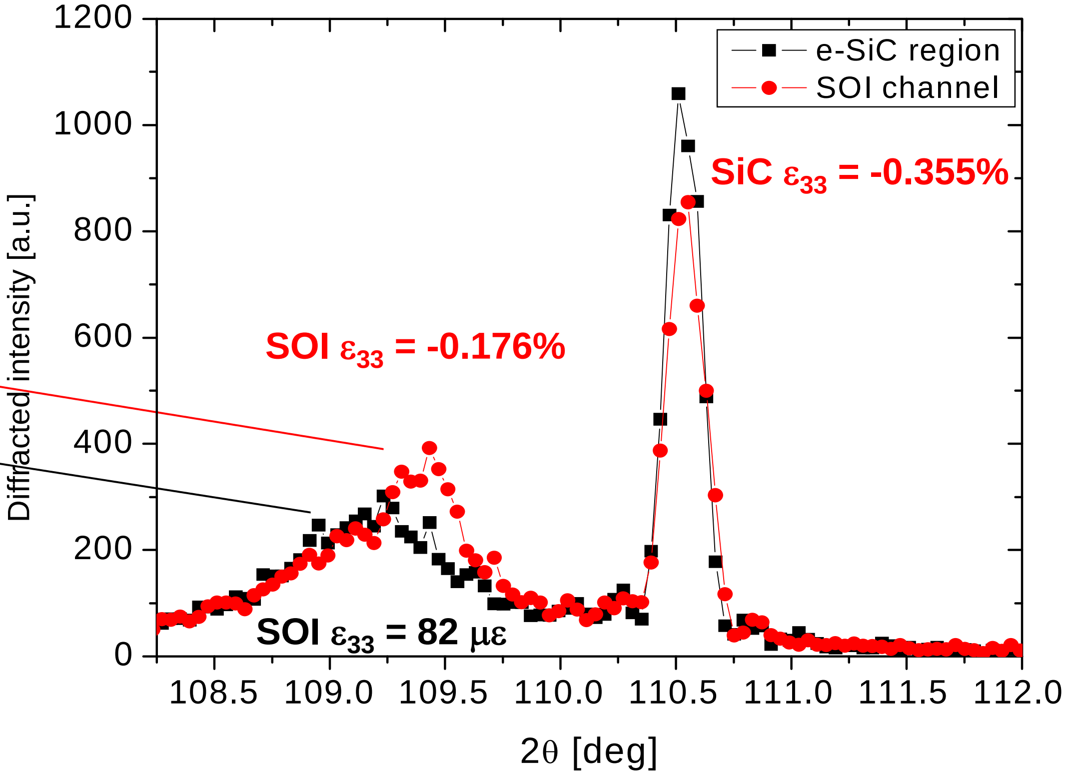
- Fresnel zone plate (FZP) optics
- E = 11.2 keV
- ~ 0.25 μm FWHM
- 0.8 mrad divergence
- ➢ map depth-averaged SOI (008)



Ex. 1: Strain in SOI channel due to embedded features

- 40 nm thick e-SiC straining 65 nm wide SOI channel (Δε = -0.472%)
- measured e-SiC strain is equivalent near SOI channel and ~ 1 μm from channel
- greater SOI strain in channel region than under e-SiC features



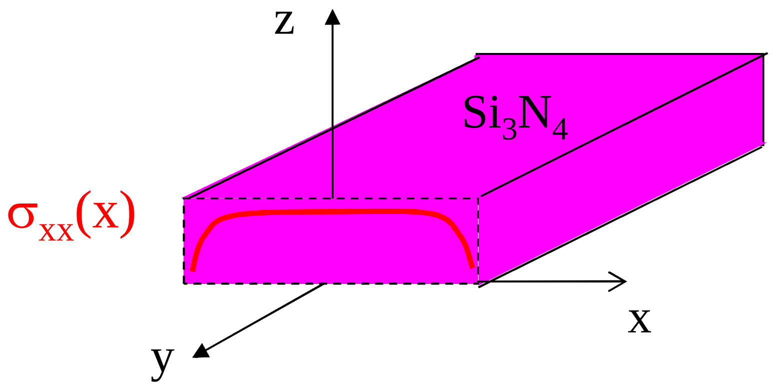


	Calc. ε_{33}	Meas. ε_{33}
e-SiC	- 0.355%	- 0.355 %
SOI	- 0.176%	- 0.167%

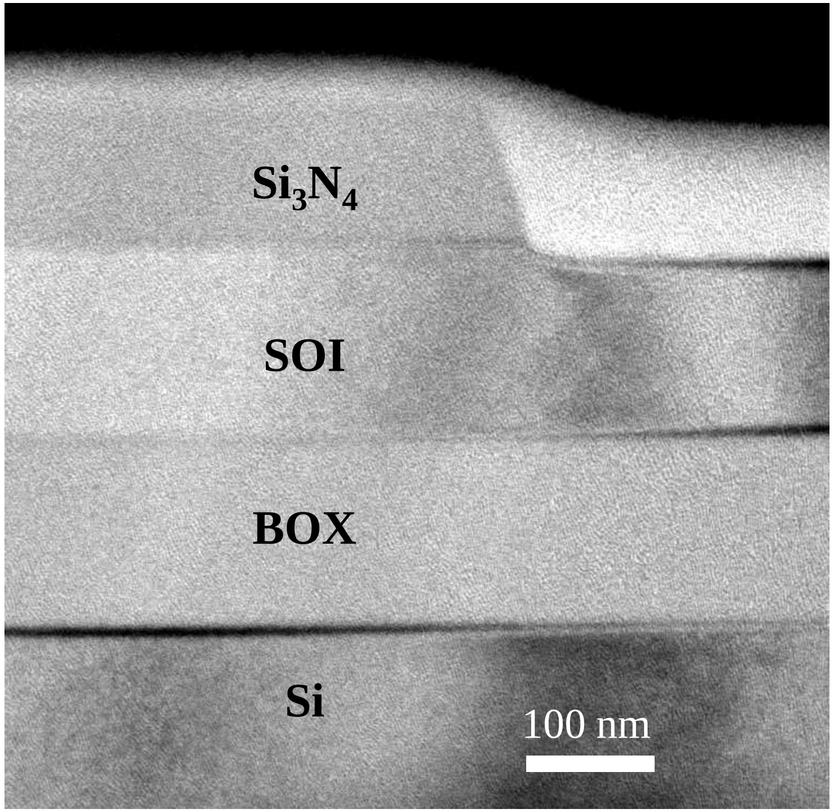
C.E. Murray et al., Appl. Phys. Lett. **94**, 063502 (2009)

- measured SOI strain ~ 95% of calculated value in SOI channel (Eshelby inclusion method)

Ex. 2: overlying stressor structures on SOI

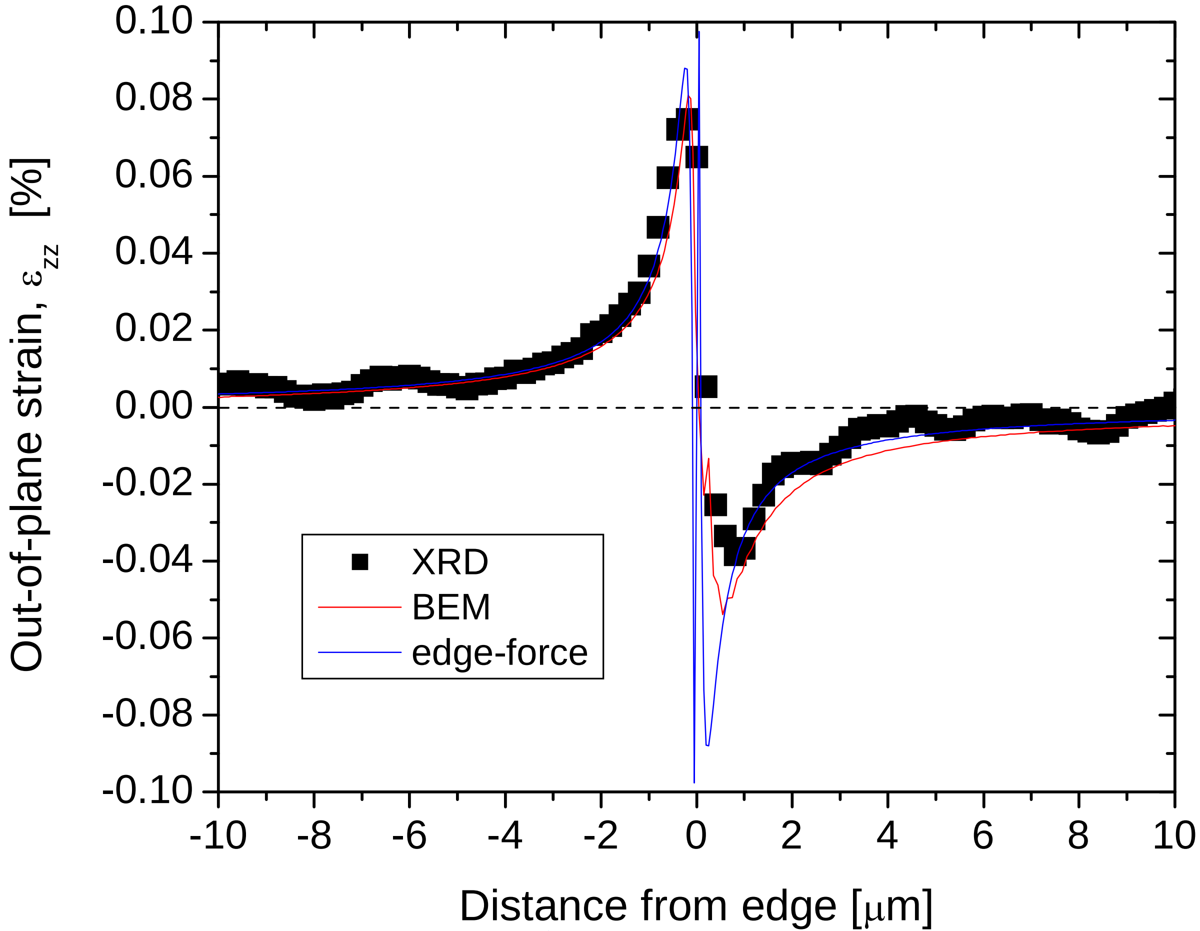


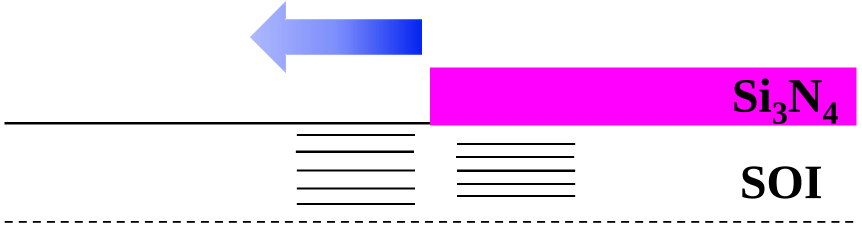
SOI (001) substrate



- stressor features fabricated from blanket Si_3N_4 films
- blanket film stress (σ_B) = -2.5 GPa (curvature)
- elastic relaxation at feature edges induces deformation in underlying layers
- investigate SOI strain distributions vs. Si_3N_4 feature width

Results: depth-averaged SOI strain (2 x 2 mm feature)





- out-of-plane strain extends ~ 4 μm (40 t) from edge
- maximum strain in SOI < 1 μm from feature edge

BEM[#] produces more accurate results than edge-force model*

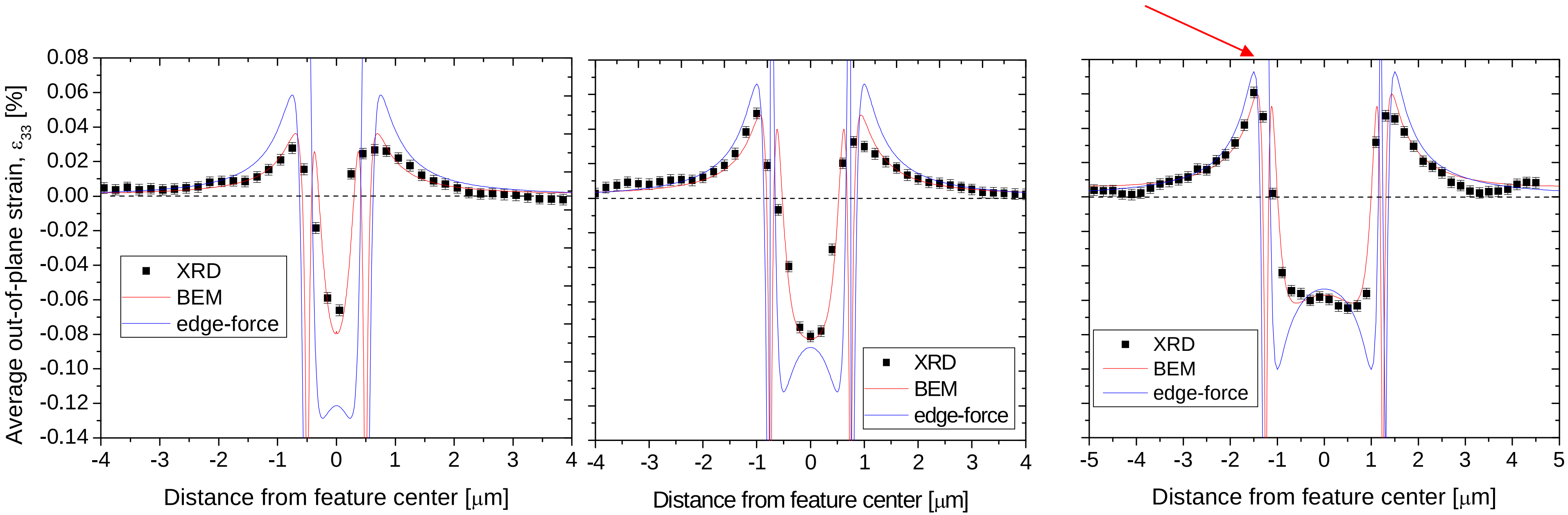
  - asymmetric strain distribution captured
  - calculated σ_B = -2.5 GPa

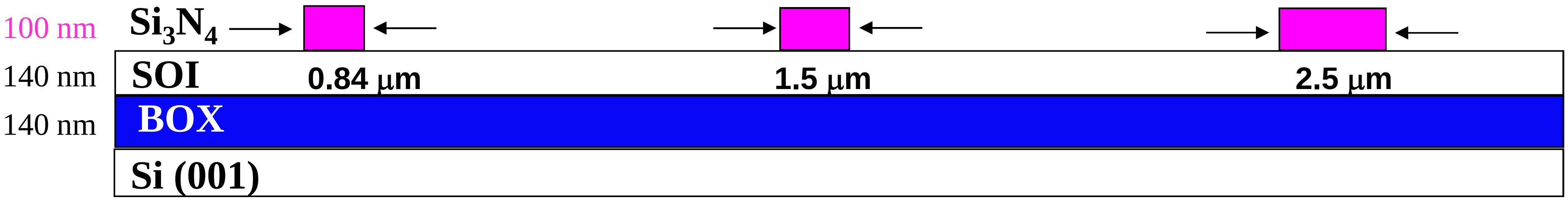
*C.E. Murray, J. Appl. Phys. **100**, 103532 (2006)

[#] C.E. Murray et al., J. Appl. Phys. **104**, 013530 (2008)

Effects of stressor size on underlying strain

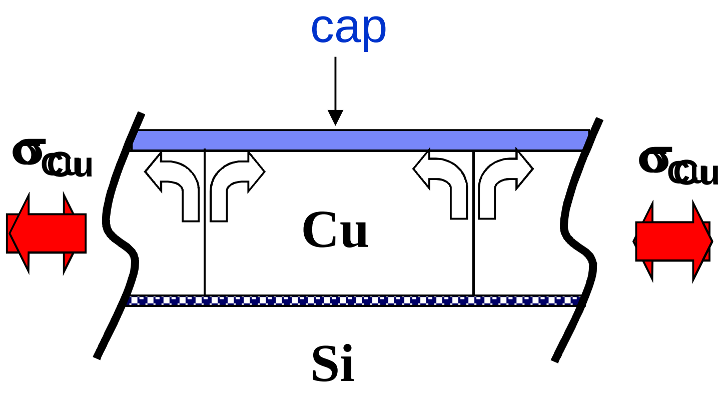
- **Si_3N_4 features: -2.5 GPa blanket film stress** (wafer curvature and microbeam XRD)
  - strain in SOI varies due to overlapping stress concentrations at edges
  - outside of features: SOI strain decreases with decreasing Si_3N_4 width

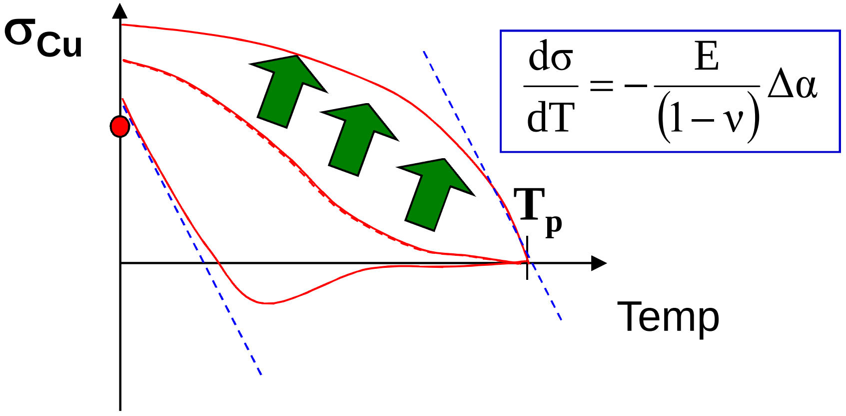




C.E. Murray et al., Thin Solid Films **530**, 85 (2013)

Processing-induced stresses in plated Cu films





$$\frac{d\sigma}{dT} = -\frac{E}{(1-\nu)}\Delta\alpha$$

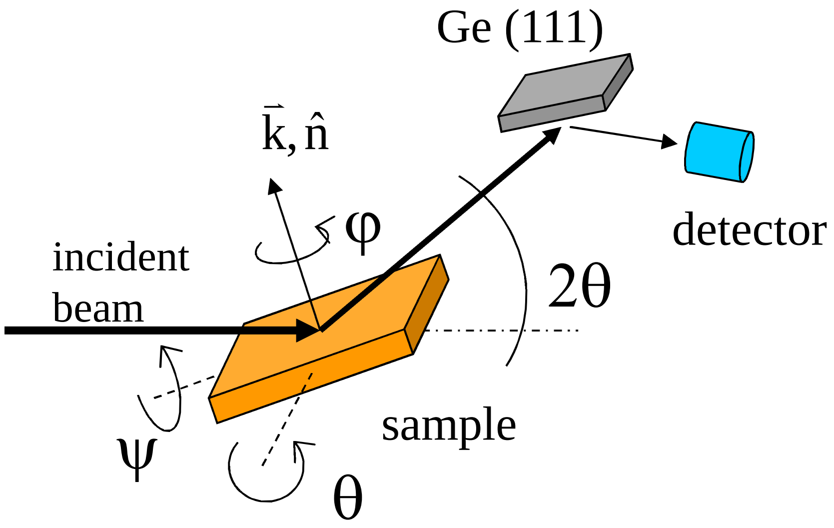
Subsequent processing exposes metallization to higher temperatures (T_p ~ 400 ^{0}C)

- free surface accommodates Cu extrusions (creep) to reduce stress as Cu film temperature decreases from process temperature, T_p:
- ➢ deviates from linear stress / strain behavior
- ➢ without plastic deformation, $\Delta T = 325\ ^0$C increases stress by ~ 900 MPa

Capping layer modifies Cu film relaxation

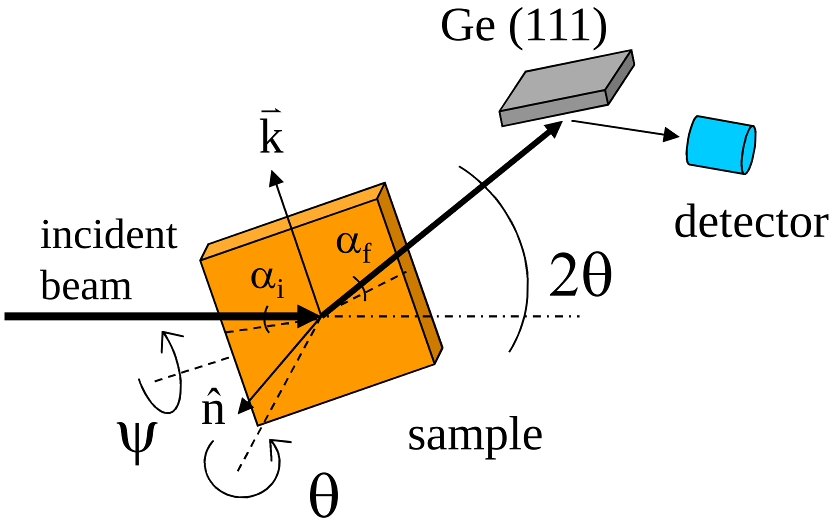
- mitigates diffusion at cap / Cu interface
- what is the impact on stress at this interface?
- ➢ exacerbate electromigration-induced voiding?

X-ray stress analysis of Cu films: diffraction geometry



Conventional XRD:

- Cu (220) reflection studied in capped, Cu films
- 21 points ($\pm \psi$) for d vs. $\sin^2(\psi)$ analysis
- σ_B and effective $d_{//}$ ($\psi = 90^0$)

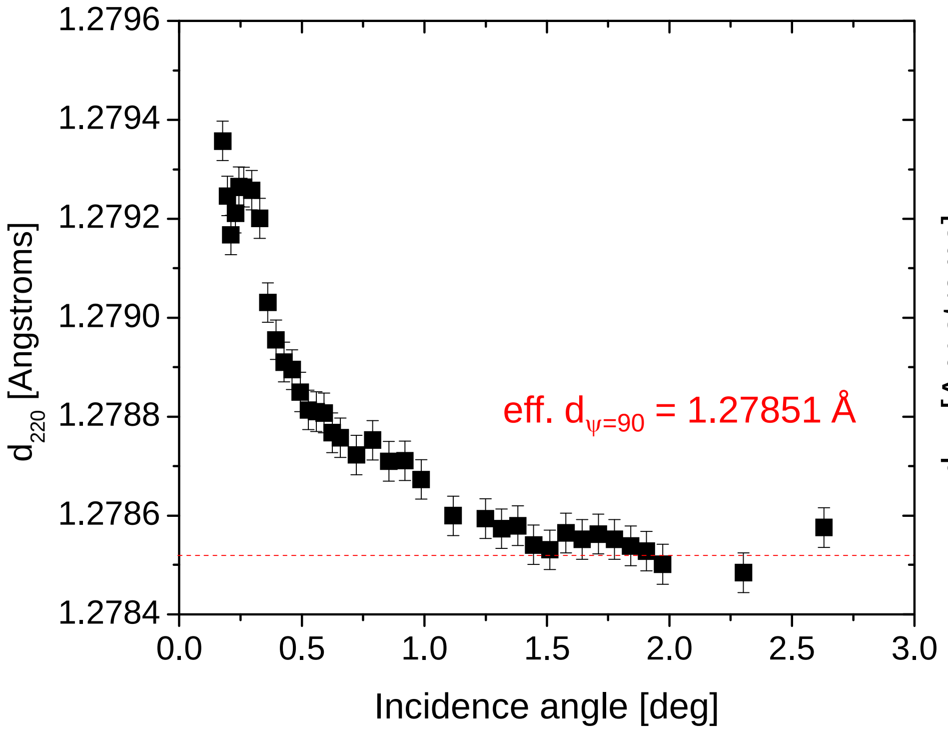


Glancing angle XRD:

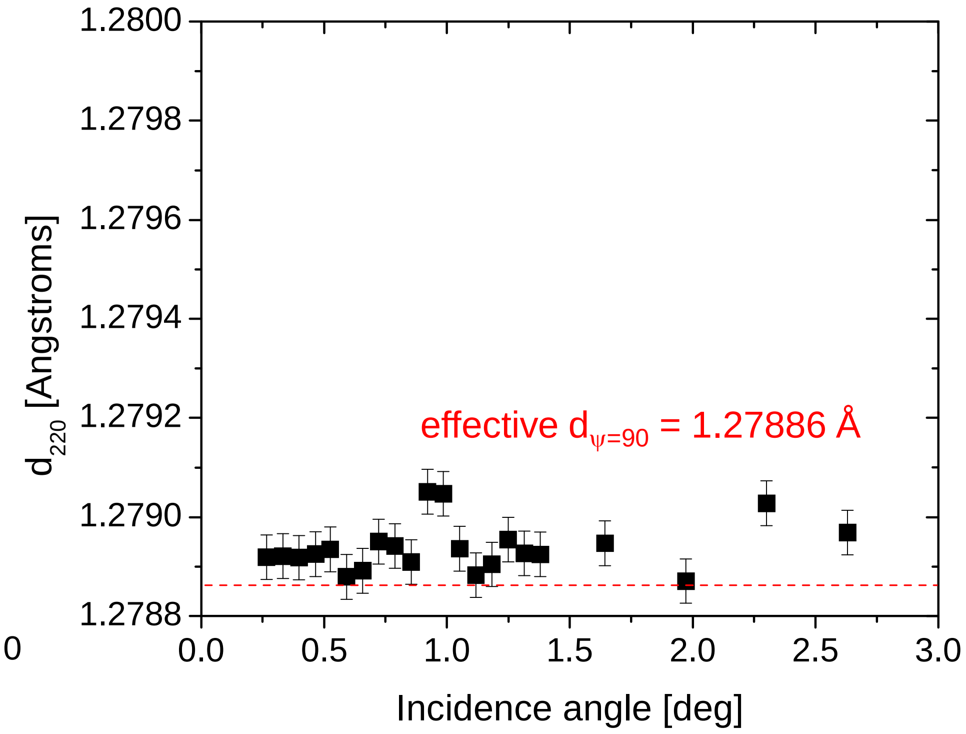
- special case of $|\psi| \sim 90^0$
- symmetric condition ($\alpha_i = \alpha_f$) mitigates refraction effects
- Cu (220) reflection vs. α_i

Results: near-surface lattice spacings

35 nm $SiC_xN_yH_z$-capped, 0.65 μm Cu film

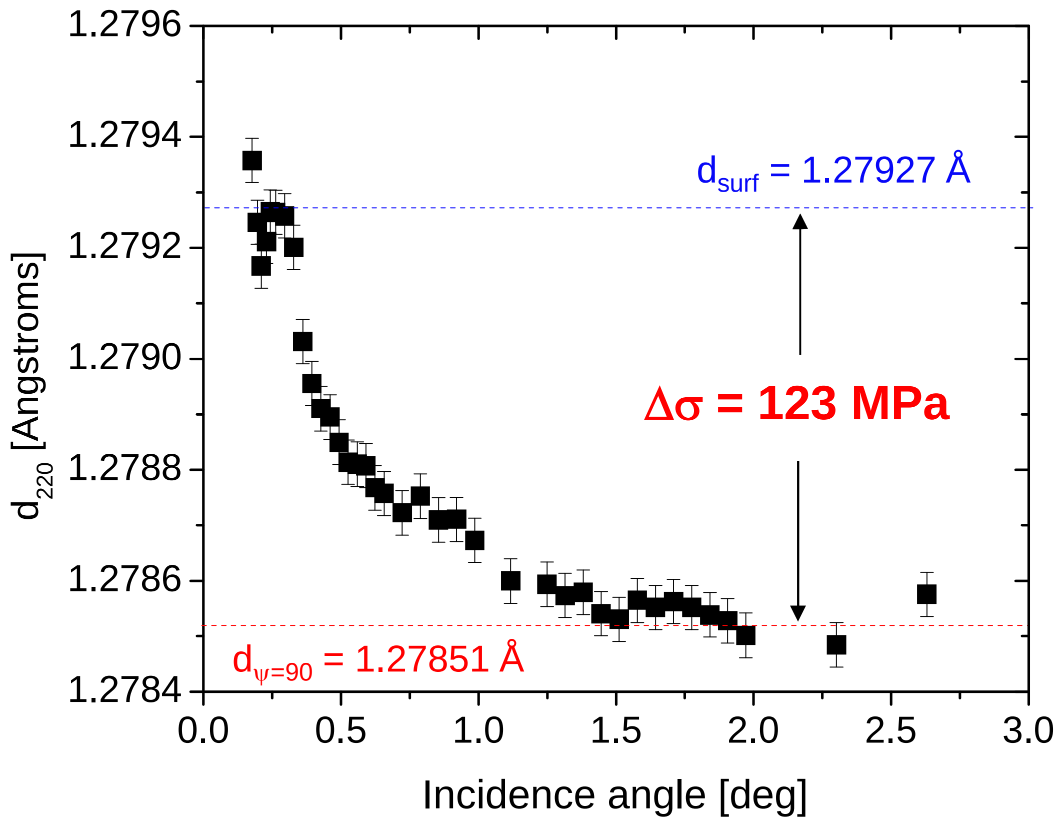


7.5 nm CoWP-capped, 0.65 μm Cu film



- Cu (220) lattice spacing is larger near Cu surface capped with $SiC_xN_yH_z$
- constraint imposed by $SiC_xN_yH_z$ cap limits top Cu surface relaxation **350 ^{0}C deposition**
- ➢ small change of in-plane lattice spacing for CoWP-capped Cu film **< 100 ^{0}C deposition**

Quantification of near-surface Cu stress



$\Delta\varepsilon_{surf}$

$$\Delta\sigma = \left(\frac{E}{1-\nu}\right)_{XEC}\left(\frac{d_{surf} - d_{\psi=90^0}}{d_{\psi=90^0}}\right)$$

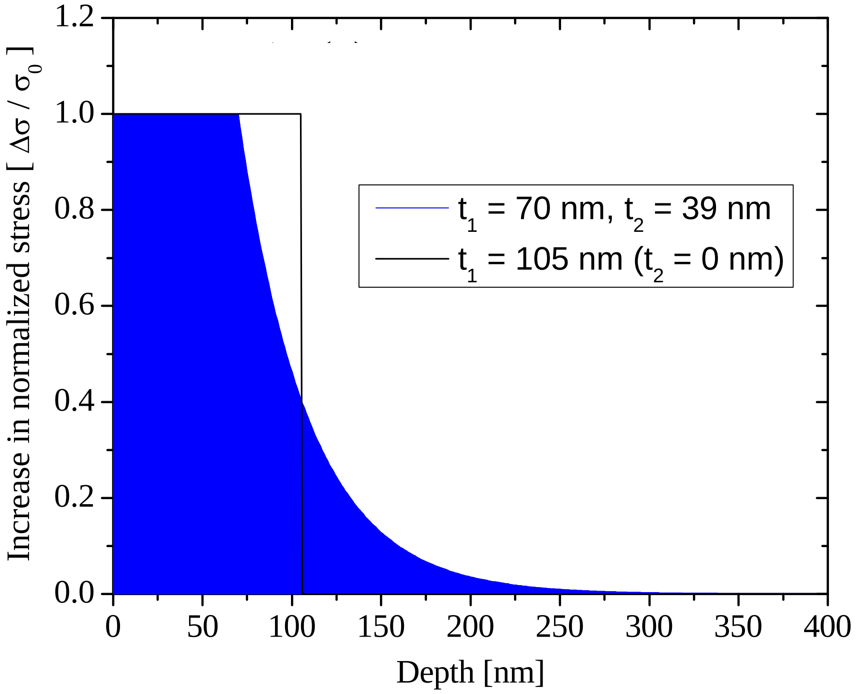
$$\left(\frac{1-\nu}{E}\right)_{XEC} = 2S_1 + \tfrac{1}{2}S_2$$

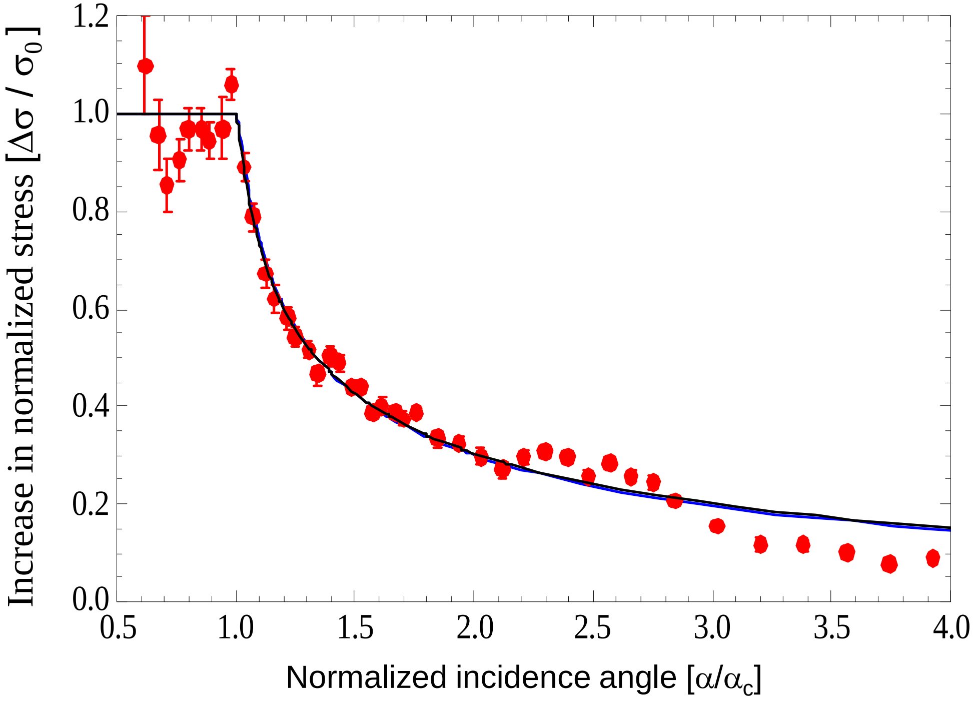
$$= 4.847\ \mathrm{TPa}^{-1}\ \text{for (220)}$$

- 85% increase of in-plane stress near cap / Cu interface
- CoWP deposition only produces elastic deformation near cap / Cu interface (Δσ < 10 MPa)

Depth-dependent stress gradients

- GIXRD measurements → convolution of stress gradient and penetration depth
- use analytic approximation of stress gradient (constant + exponential decay)





- least-squares fitting of (220) data from $SiC_xN_yH_z$-capped, 2.2 μm Cu film

➢ gradient extends 100 to 200 nm below interface

C.E. Murray, Appl. Phys. Lett. **104**, 081920 (2014)

Summary and Conclusions

- Feature geometry impacts strain in nanoelectronic features
  - strain distributions can extend 40 x film thickness
  - interfacial integrity → key to strain transfer by elastic relaxation
  - increasing device density → decreasing stressor volume
- Complementary characterization techniques are essential
  - bridging different length-scales (cm → nm)
  - investigation of 3D strain distributions is needed to understand interaction among **all** components
- Stress gradients induced in Cu-based metallization
  - $SiC_xN_yH_z$ capping limits Cu plastic relaxation
  - capping at lower temperatures produces elastic deformation → no gradient

Acknowledgments

IBM:

- Z. Ren
- J. Holt
- G. Cohen
- K. Saenger
- J. Jordan-Sweet

Argonne National Laboratory:

- Z. Cai

This work was performed by the Research Alliance Teams at various IBM Research and Development facilities.

U.S. DOE, Office of Science, Office of Basic Energy Sciences, Contract No.'s DE-AC02-06CH1135, DE-AC02-06CH11357.